

ABSTRACT OF THE DISCLOSURE

The present invention relates to a synchronous self timed memory device. The device includes a plurality of memory cells forming a cell array, at least one local decoder interfacing with the cell array, at least one local sense amplifier and at least one local controller. The local sense amplifier interfaces with at least the decoder and cell array, and is adapted to precharge and equalize at least one line coupled thereto. The local controller interfaces with and coordinates the activities of at least the local decoder and sense amplifier.